* 1. 0x00000020, cacheable, data ram
  2. 0x00000020, non-cacheable, data ram
  3. 0x1F800001, non-cacheable, sfrs
  4. 0x1FC00111, cacheable, bootflash
  5. 0x1D001000, cacheable, program flash

3. a.

Port B: 0 -15

Port C: 12-15

Port D: 0-11

Port E: 0-7

Port F: 0,1,3,4,5

Port G: 2,3,6,7,8,9

Pin 60

b. 5-7,11,13-15,17-31

7. The processor.o file has more information than what is necessary to run on the pic32 so when the program is compiled into a hex executable it is stripped down to just what the pic needs to run which is much smaller.

8. a.

\_start\_bss\_init:

la t0,\_bss\_begin

la t1,\_bss\_end

b \_bss\_check

nop

\_bss\_init:

sw zero,0x0(t0)

addu t0,4

\_bss\_check:

bltu t0,t1,\_bss\_init

nop

#if defined(INIT\_L1\_CACHE) || defined(\_\_PIC32\_HAS\_L1CACHE)

b.

ffffffffbf88cb4c A C2FIFOCI31INV

ffffffffbfc02ff0 A DEVCFG3

ffffffffbfc02ff4 A DEVCFG2

ffffffffbfc02ff8 A DEVCFG1

ffffffffbfc02ffc A DEVCFG0

c. SPIRBF 1, SPITBF 1, SPITBE 1, SPIRBE 1, SPIROV 1, SRMT 1, SPITUR 1, SPIBUSY 1, TXBUFELM 5, RXBUFELM 5

9.

TRIDSET = 0xc

TRISDCLR = 0x22

TRISDINV = 0X11